AMENDMENTS TO THE SPECIFICATION

Please substitute the following replacement paragraphs for like-numbered paragraphs of the specification:

[0015] During a read or write operation within the CAM device 100, the address decoder 105 receives an address from the address bus 104 (or from an address source within the CAM device 100) and activates a corresponding one of word lines 112 to access a row of CAM cells. In a read operation, each of the ternary CAM cells within the accessed row outputs the bits of the stored bit pair onto the bit lines 116, thereby enabling the ternary CAM word to be read out via the data port (i.e., amplified by sense amplifier circuitry within the read/write circuit 103 and output onto the data bus 106). Conversely, in a write operation, write driver circuitry within the read/write circuit outputs a write data value onto the bit line pairs to store an entry, including the aforementioned compound entry, within the accessed row of ternary CAM cells. In one embodiment, two pairs of bit lines are provided to each column of CAM cells to enable the corresponding bit pair of a ternary CAM word to be read or written in a single access ~~operation~~ operation. In an alternative embodiment, a single pair of bit lines may be provided per CAM cell column to enable time-multiplexed access to the ternary CAM word (i.e., bits of a given bit pair transferred one after the other). In such an embodiment, two word lines 112 may be provided for each row of CAM cells, one to enable access to a first bit (e.g., a data bit) and the other to enable access to a second bit (e.g., a mask bit) within each CAM cell of the row. In another alternative embodiment, the bit lines may be omitted altogether, and the compare lines used in time-multiplexed fashion for either read/write access or search key delivery.

[0018] Figure 2 is a flow diagram for writing a compound entry at a specified address within the ternary CAM device of Figure 1. Initially, at block 201, the host device obtains a ternary CAM word (e.g., by extracting selected bits from a packet or packet header and/or by obtaining a mask value). At block 203, the host device generates the

mask specifier based on the mask component of the ternary CAM word. At block 205, the host device issues a write instruction to the CAM device together with the specified address, ternary CAM word and mask specifier, thus instructing the CAM device to write a compound entry (i.e., formed by the ternary CAM word and mask specifier) into the address-specified row of ternary CAM cells. The ternary CAM word and mask specifier may be provided to the CAM device in a single transfer operation or in a sequence of one or more transfers, depending on the width of the compound entry and the width of the bus used to deliver the compound entry to the CAM device. Also, in an alternative embodiment, the generation of the mask specifier may be performed by the CAM device itself rather than the host device. Such an embodiment is described below in further detail. Further, rather than obtaining a ternary CAM word at block 201, the host device may obtain a data field component of the ternary CAM word and an encoded mask value (e.g., a prefix in an internet protocol (IP) such as ~~and~~ an IPv4 prefix or an IPv6 prefix that indicates the number of most-significant-bits of the data field component that are to be unmasked and, by implication, the number of least-significant bits of the data field component that are to be masked). The host device may deliver the encoded mask value to the CAM device at block 205, with the CAM device itself generating the mask field component of the ternary CAM word therefrom.

[0025] The CAM cell 330 includes a first storage element 331 to store the 'X' bit of the XY conversion result, and a second storage element 333 to store the 'Y' bit of the XY conversion result, together with a compare circuit formed by transistors Q1, Q2, Q3 and Q4. Transistors Q1 and ~~Q2~~ Q3 are coupled to receive the C and /C bits, respectively (i.e., complementary representation of a search key bit, S), and transistors ~~Q3~~ Q2 and Q4 are coupled to receive the X bit and Y bit from the storage elements 331 and 333 respectively. Referring to the XY conversion logic of table 1, and Figure 7, when the mask bit is in a masking state (e.g., a '1'), then both the X and Y bits are '0', thereby switching off transistors Q2 and Q4 and isolating the match line (ML) from ground (i.e., at least within the CAM cell 330). When the mask bit is in the non-masking state, then the X and Y bits constitute a complementary representation of the data bit in which X =

/D and Y=D. Consequently, when the mask bit is in the non-masking state, and the search key bit does not match the data bit, then the match line will be discharged either through transistors Q1 and Q2 (i.e., S=1 and D=0, so that C=1 and X=1) or through transistors Q3 and Q4 (i.e., S=0 and D=1, so that /C=1 and Y=1). When the search key bit does match the data bit, then at least one transistor in pair Q1/Q2 and in pair Q3/Q4 is switched off, thereby preventing the CAM cell from discharging the match line.